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TESLA 3A DIS M/B Schematics Document

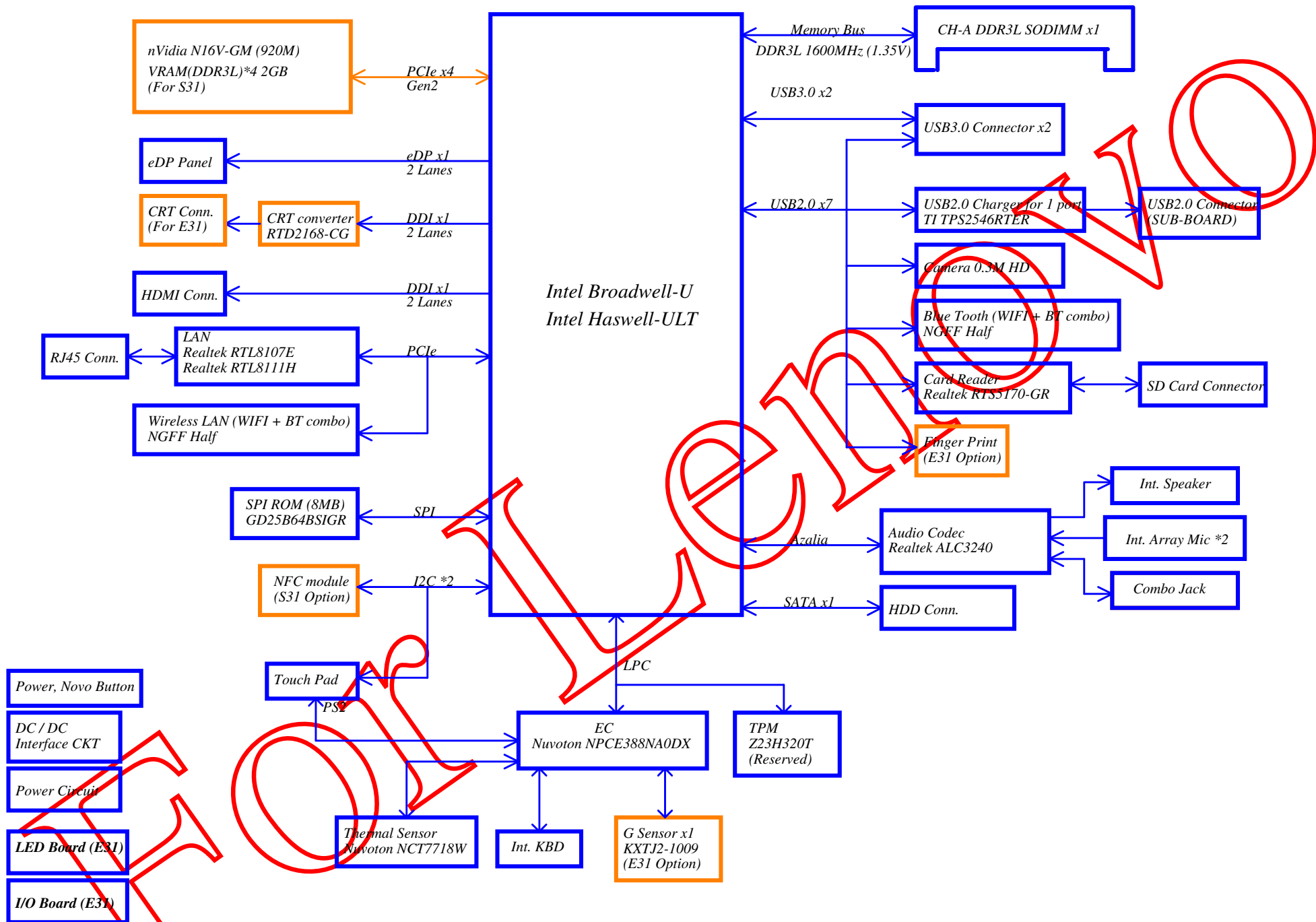
Intel Broadwell U Processor with DDR3L
Nvidia N16V-GM(920M)

2014-09-26

LA-C311P

REV : 0.1

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Voltage Rails

power plane	State	+B	+5VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0		○	○	○	○
S3		○	○	○	×
S5 S4/AC		○	○	×	×
S5 S4/ Battery only		○	×	×	×
S5 S4/AC & Battery don't exist		×	×	×	×

USB Port Table

USB 2.0	Port	3 External USB Port
EHCI1	0	USB Port USB3.0
	1	USB Port USB3.0
	2	
	3	Camera
	4	
	5	
EHCI2	6	
	7	
	8	NGFF(BT)
	9	USB Port (Charge)
	10	NGFF(WLAN)
	11	Card Reader
	12	
	13	

BOM Structure Table

Item	BOM Structure
LAN 10/100 Transformer	100@
LAN GIGA Transformer	GIGA@
LAN RTL8111H	8111H@
WLAN Support ISCT	ISCT@
WLAN No Support ISCT	NoISCT@
For Green CLK	GCLK@
For No Green CLK	NoGCLK@
For DIS	DIS@
For TPM	TPM@
For Camera	CMOS@
For NFC Option	NFC@
For ST APS	SSST@
For Bosch APS	GSB@
For E31 PWR Button ESD	EE31ESD@
For FP Option	FP@
For Green clock with DIS	GCLKDIS@
For Green clock with WMA	GCLKUMA@
For U31 Option	U31@
For E31 Option	E31@
Connector	ME@
No EMI	@EMI@
No ESD	@ESD@
For Ramix Memory	H2G@
For Samsung Memory	S2G@
For Micron Memory	M2G@

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x 16h

EC SM Bus2 address

Device	Address
NCT77718W BMA250E	1001 100x 98h 0001 100x 18h

ME SM Bus address

Device	Address
NFC	0010 1000 28h

PCH SM Bus address

Device	Address
DDR_JDIMM1 Touch Pad	1010 000x A0h

GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111x 9Eh

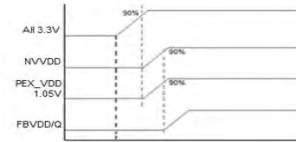
SMBUS Control Table

	SOURCE	VGA	BATT	NECP388	SODIMM	WLAN	Thermal Sensor	DGPU	NFC	TP	PCH
SMB_EC_CK1 SMB_EC_DA1	NECP388 +3VALW	×	√ +3VALW	×	×	×	×	×	×	×	×
SMB_EC_CK2 SMB_EC_DA2	NECP388 +3VS	√ +3VGS	×	√ +3VS	×	×	√ +3VS	×	×	√ +3VS	√ +3V_PCH
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW	×	×	×	√ +3VS	√ +3VS	×	×	×	×	×
SMLOCLK SML0DATA	PCH +3VALW	×	×	×	×	×	×	×	√ +3VS	×	×
SML1CLK SML1DATA	PCH +3VALW	×	×	×	×	×	×	√ +3VS	×	×	×

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	AVAILW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

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GPU Power Sequence



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Figure 3-6. Example of Power-up Sequencing Order

Note:

- The ramp time for any rail must be more than 40 μ s and is recommended to be less than 2ms.

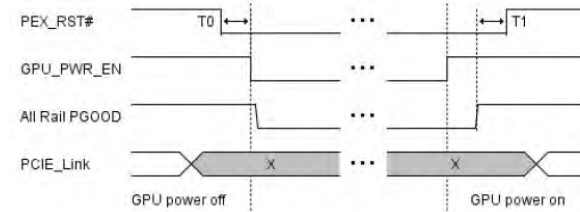
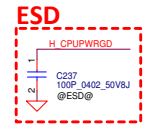
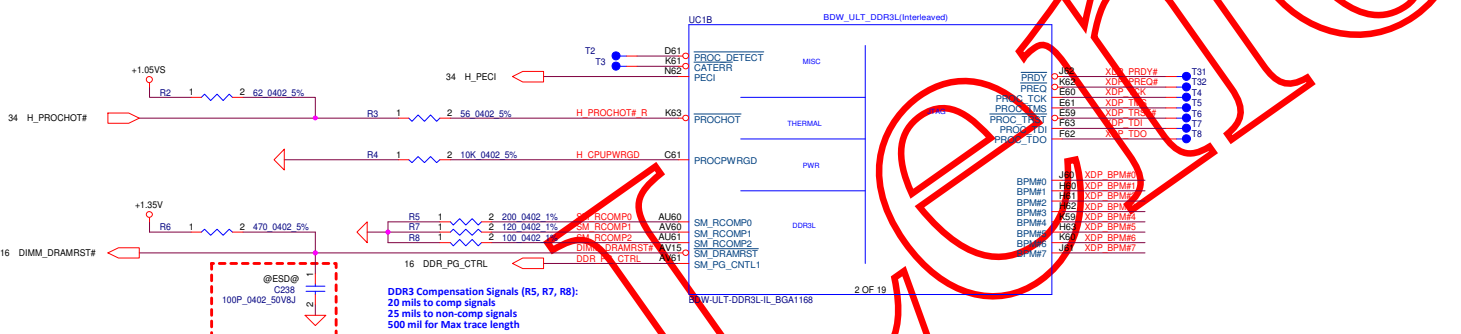
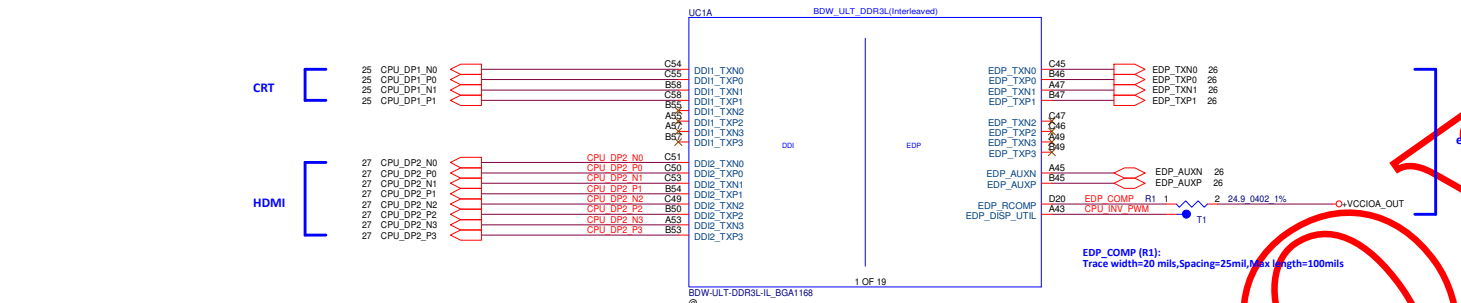


Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms



ESD

- UC1 SA00007M750 S IC CL8064701477301 QEAF D0 2G BGA C38 I7_4510U@
- UC1 SA00007L010 S IC CL8064701477802 QEAK D0 1.7G BGA I5_4210U@
- UC1 SA00007TX10 S IC CL8064701553300 QEZA D0 2G BGA 1168 I3_4120U@
- UC1 SA00007TA10 S IC CL8064701552900 QEZ6 D0 1.9G BGA I3_4030U@
- UC1 SA00007TW10 S IC CL8064701553401 QEZB D0 1.9G C38 I3_4025U@
- UC1 SA00007G030 Intel 2957U 1.4G 2M D0 2: BGA CPU 2957U@
- UC1 SA00007G230 S IC CL8064701569500 QFAN D0 1.7G BGA 3558U@
- UC1 SA00006SLA0 S IC CL8064701477202 QEVD C0 1.8G BGA I7_4500U@
- UC1 SA00006SMC0 S IC CL8064701477702 SR170 C0 1.6G C38 I5_4500U@
- UC1 SA00007AM00 S IC CL8064701614813 QFSY C0 1.6G BGA QFSY@
- UC1 SA00006SLU30 S IC CL8064701476302 SR16P C0 1.8G C38 I3_4100U@
- UC1 SA000072C50 S IC CL8064701478404 QEAR D0 1.7G C38 I3_4005U@
- UC1 SA00006SX80 S IC CL8064701478202 SR16Q C0 1.7G C38 I3_4010U@

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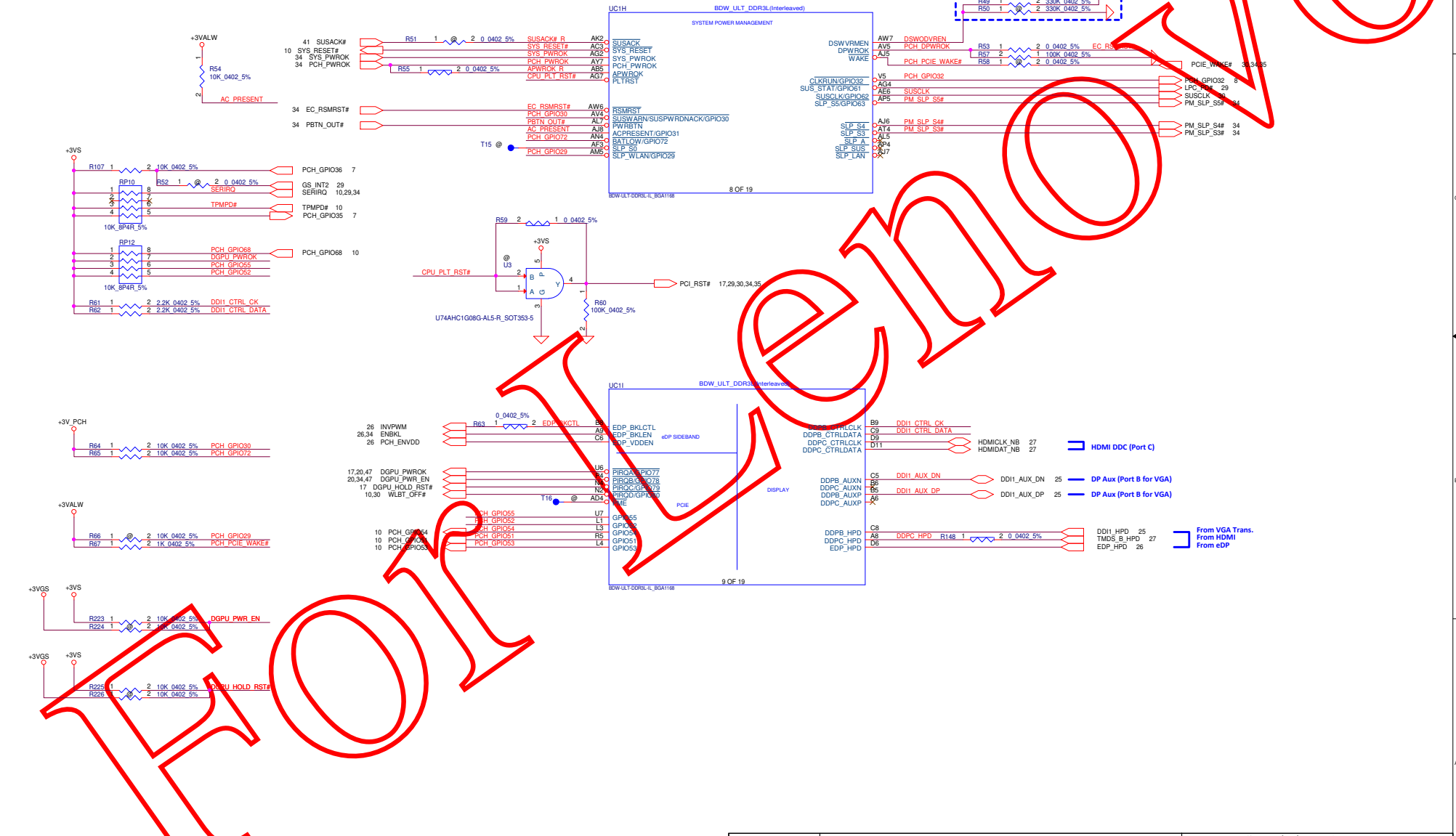
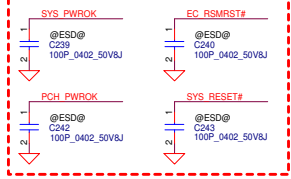
Interleaved Memory



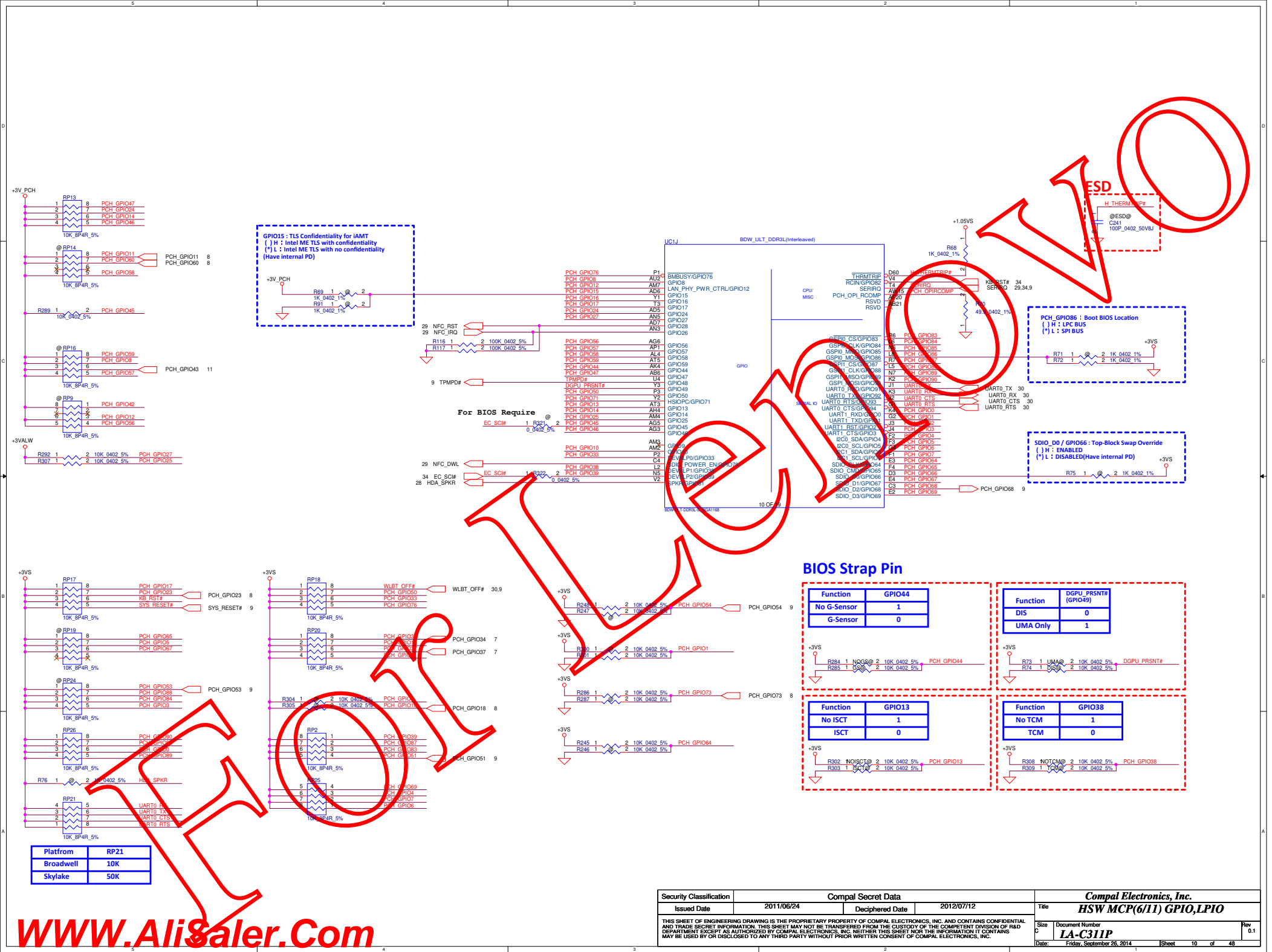
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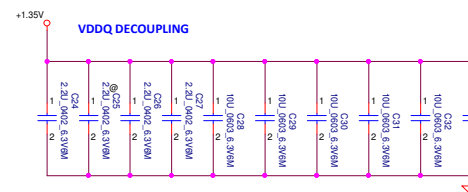
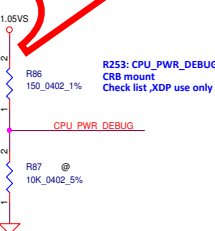
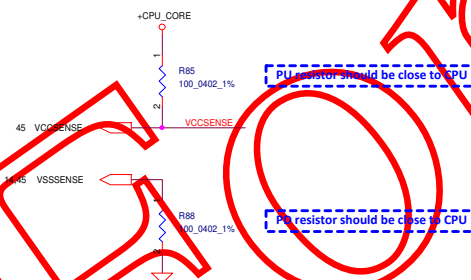
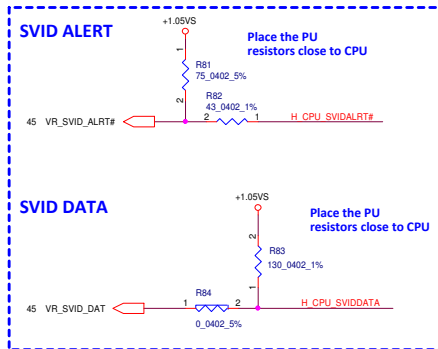
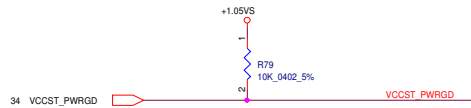
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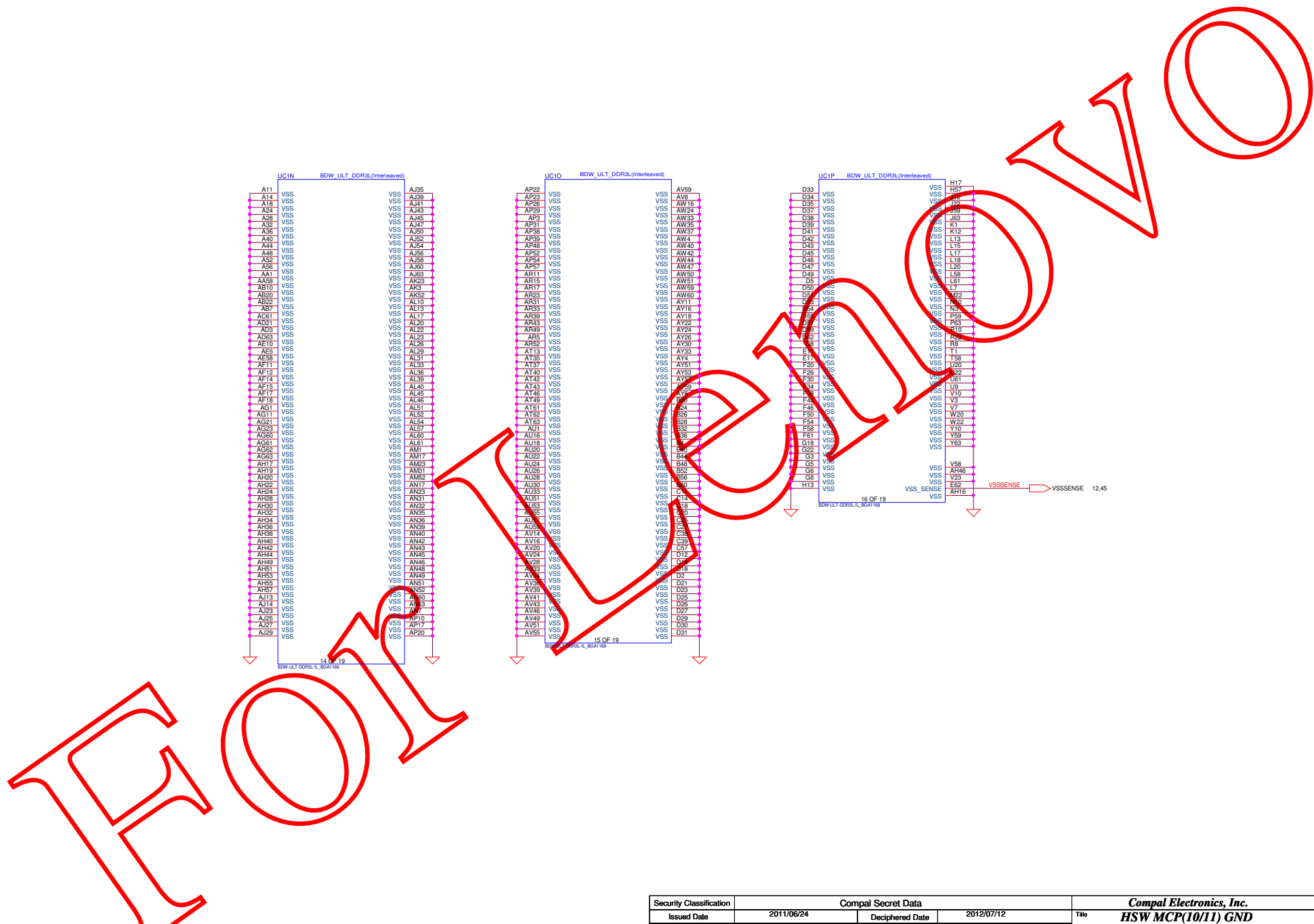
ESD



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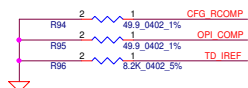
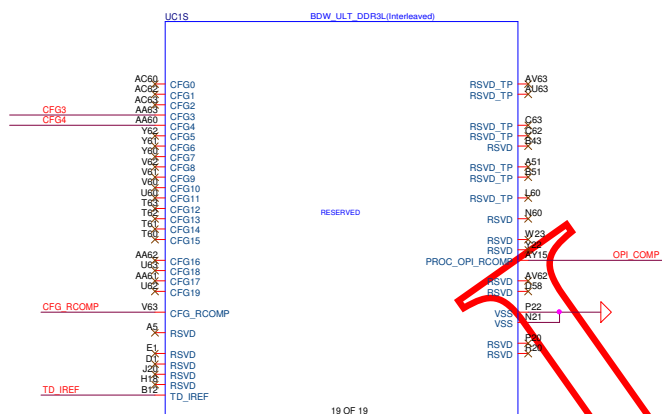
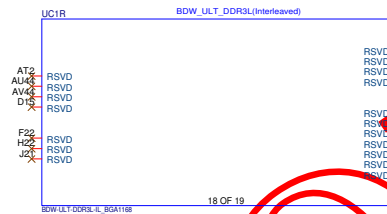
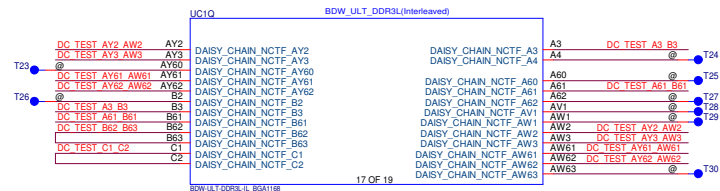


UC1N BOW ULT_DDR3L(Interleaved)			UC10 BOW ULT_DDR3L(Interleaved)			UC1P BOW ULT_DDR3L(Interleaved)			H17		
A11	VSS	AJ35	AP22	VSS	AV59	D33	VSS	H17	VSS		
A14	VSS	AJ39	AP23	VSS	AV8	D34	VSS	H19	VSS		
A18	VSS	AJ41	AP26	VSS	AW16	D35	VSS	H20	VSS		
A24	VSS	AJ43	AP29	VSS	AW24	D37	VSS	H22	VSS		
A28	VSS	AJ45	AP3	VSS	AW33	D38	VSS	H23	VSS		
A32	VSS	AJ47	AP31	VSS	AW35	D39	VSS	H24	VSS		
A36	VSS	AJ50	AP38	VSS	AW37	D41	VSS	H25	VSS		
A40	VSS	AJ52	AP39	VSS	AW4	D42	VSS	H26	VSS		
A44	VSS	AJ54	AP46	VSS	AW40	D43	VSS	H27	VSS		
A48	VSS	AJ55	AP50	VSS	AW42	D45	VSS	H28	VSS		
A52	VSS	AJ58	AP54	VSS	AW44	D46	VSS	H29	VSS		
A56	VSS	AJ60	AP57	VSS	AW47	D47	VSS	H30	VSS		
A60	VSS	AJ63	AR11	VSS	AW50	D49	VSS	H31	VSS		
AX58	VSS	AK23	AR15	VSS	AW51	D5	VSS	H32	VSS		
AB10	VSS	AK3	AR17	VSS	AW59	D50	VSS	H33	VSS		
AB20	VSS	AK52	AR23	VSS	AW60	D51	VSS	H34	VSS		
AB22	VSS	AL10	AR31	VSS	AV11	D52	VSS	H35	VSS		
AB7	VSS	AL13	AR33	VSS	AV16	D53	VSS	H36	VSS		
AD21	VSS	AL17	AR39	VSS	AV18	D54	VSS	H37	VSS		
AD21	VSS	AL20	AR43	VSS	AV22	D55	VSS	H38	VSS		
AD3	VSS	AL22	AR49	VSS	AV24	D56	VSS	H39	VSS		
AD53	VSS	AL23	AR5	VSS	AV26	D57	VSS	H40	VSS		
AE10	VSS	AL28	AR52	VSS	AV30	D58	VSS	H41	VSS		
AES	VSS	AL29	AT13	VSS	AV33	D59	VSS	H42	VSS		
AE58	VSS	AL31	AT35	VSS	AV4	D6	VSS	H43	VSS		
AF11	VSS	AL33	AT37	VSS	AV51	D60	VSS	H44	VSS		
AF12	VSS	AL36	AT40	VSS	AV53	D61	VSS	H45	VSS		
AF14	VSS	AL38	AT42	VSS	AV54	D62	VSS	H46	VSS		
AF15	VSS	AL40	AT43	VSS	AV59	D63	VSS	H47	VSS		
AF17	VSS	AL43	AT46	VSS	AV69	D64	VSS	H48	VSS		
AF18	VSS	AL46	AT49	VSS	AV74	D65	VSS	H49	VSS		
AG1	VSS	AL51	AT61	VSS	AV8	D66	VSS	H50	VSS		
AG11	VSS	AL52	AT62	VSS	AV8	D67	VSS	H51	VSS		
AG21	VSS	AL54	AT63	VSS	AV8	D68	VSS	H52	VSS		
AG23	VSS	AL57	AT1	VSS	AV8	D69	VSS	H53	VSS		
AG59	VSS	AL60	AT16	VSS	AV8	D70	VSS	H54	VSS		
AG61	VSS	AL61	AT18	VSS	AV8	D71	VSS	H55	VSS		
AG62	VSS	AM1	AT20	VSS	AV8	D72	VSS	H56	VSS		
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AH20	VSS	AM52	AT28	VSS	AV8	D76	VSS	H60	VSS		
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AH24	VSS	AN23	AT33	VSS	AV8	D78	VSS	H62	VSS		
AH26	VSS	AN31	AT35	VSS	AV8	D79	VSS	H63	VSS		
AH30	VSS	AN32	AT35	VSS	AV8	D80	VSS	H64	VSS		
AH32	VSS	AN35	AT35	VSS	AV8	D81	VSS	H65	VSS		
AH34	VSS	AN38	AT35	VSS	AV8	D82	VSS	H66	VSS		
AH36	VSS	AN39	AT35	VSS	AV8	D83	VSS	H67	VSS		
AH38	VSS	AN40	AT35	VSS	AV8	D84	VSS	H68	VSS		
AH40	VSS	AN42	AT35	VSS	AV8	D85	VSS	H69	VSS		
AH42	VSS	AN43	AT35	VSS	AV8	D86	VSS	H70	VSS		
AH44	VSS	AN45	AT35	VSS	AV8	D87	VSS	H71	VSS		
AH49	VSS	AN46	AT35	VSS	AV8	D88	VSS	H72	VSS		
AH51	VSS	AN48	AT35	VSS	AV8	D89	VSS	H73	VSS		
AH53	VSS	AN49	AT35	VSS	AV8	D90	VSS	H74	VSS		
AH55	VSS	AN51	AT35	VSS	AV8	D91	VSS	H75	VSS		
AH57	VSS	AN52	AT35	VSS	AV8	D92	VSS	H76	VSS		
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AJ13	VSS	AP3	AT35	VSS	AV8	D94	VSS	H78	VSS		
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AJ23	VSS	AP7	AT35	VSS	AV8	D96	VSS	H80	VSS		
AJ25	VSS	AP7	AT35	VSS	AV8	D97	VSS	H81	VSS		
AJ27	VSS	AP17	AT35	VSS	AV8	D98	VSS	H82	VSS		
AJ29	VSS	AP20	AT35	VSS	AV8	D99	VSS	H83	VSS		
AJ29	VSS		AT35	VSS	AV8	D100	VSS	H84	VSS		

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BOW ULT_DDR3L(Interleaved)

VSSsense 12.45

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CFG Straps for Processor

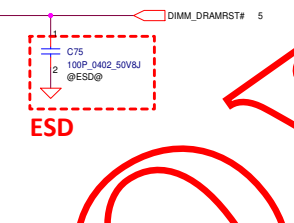
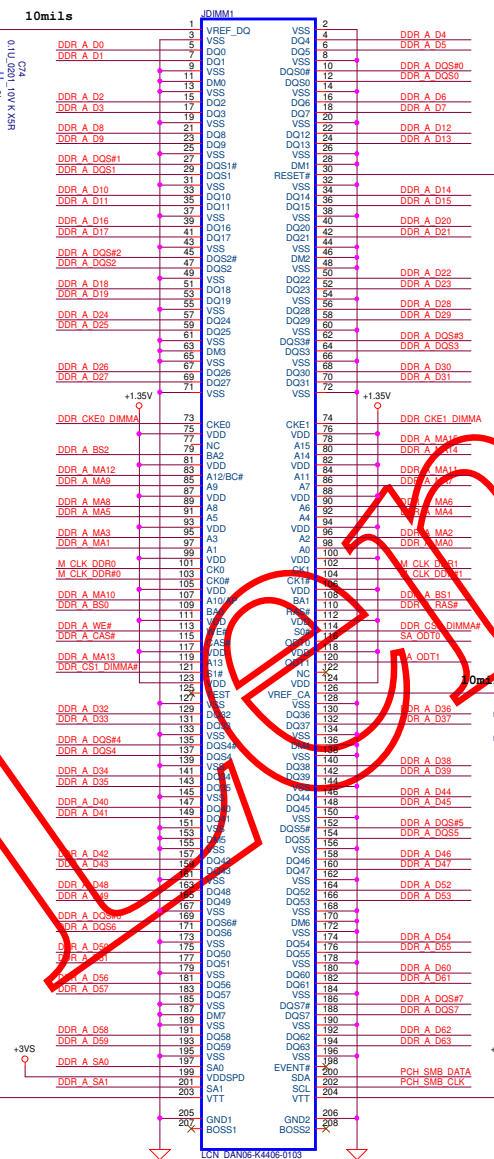
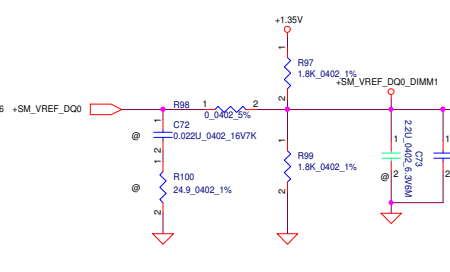
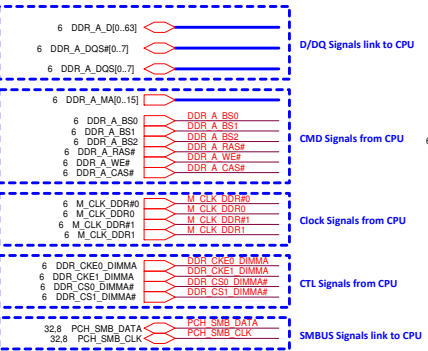
Physical Debug Enable (DFX Privacy)

CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
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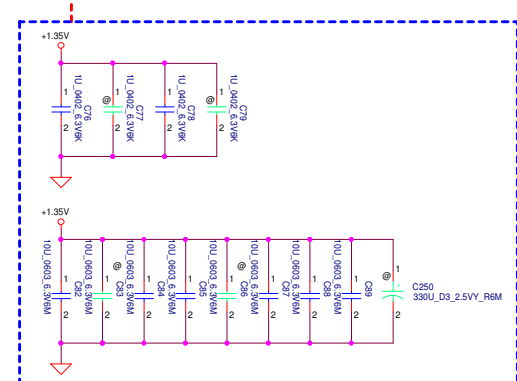
Display Port Presence Strap

CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port
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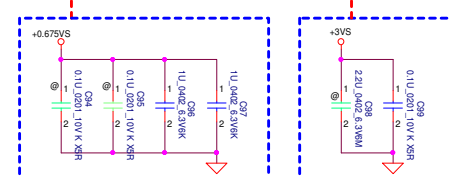
DIMM1 Dimmer Type Near CPU



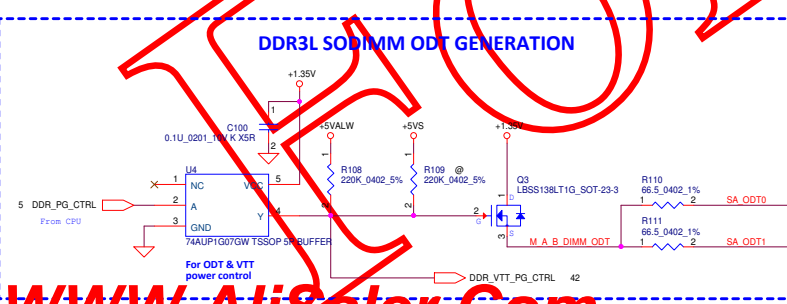
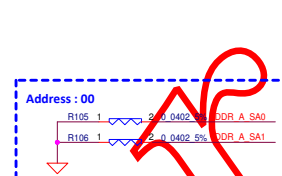
Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203,204

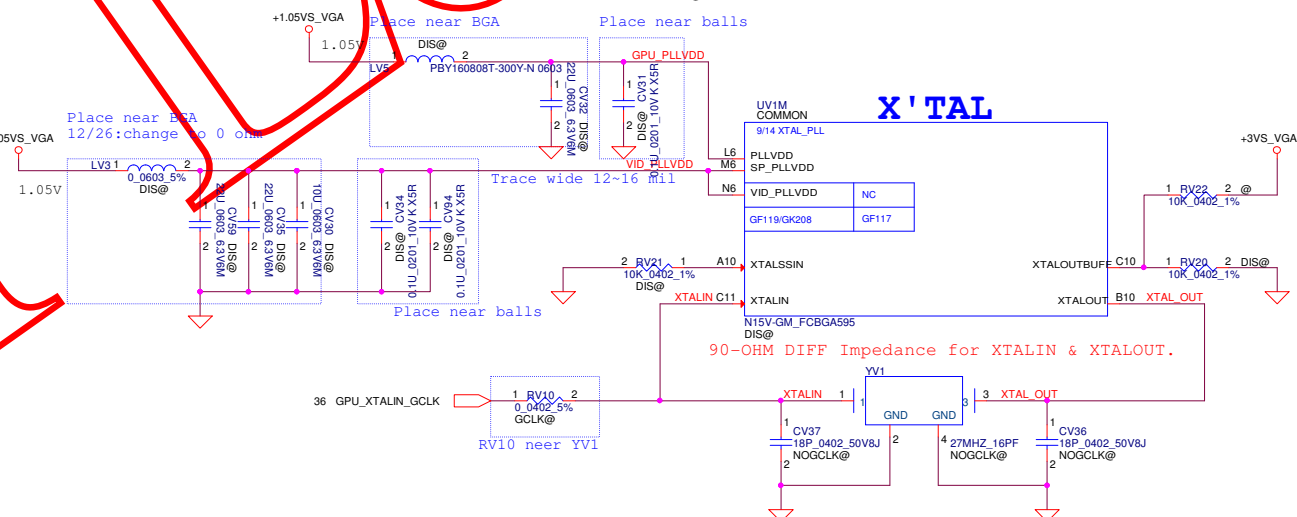
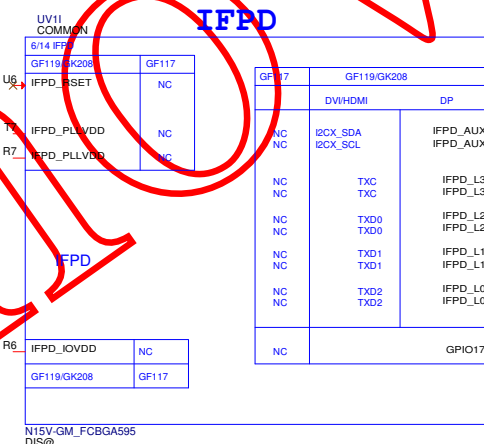
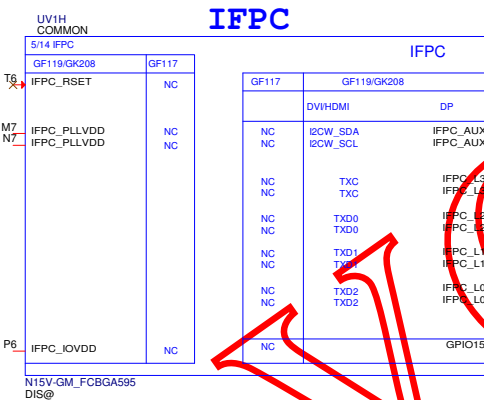
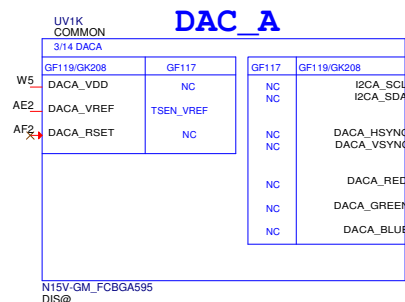


Layout Note:
Place near JDIMM1.199

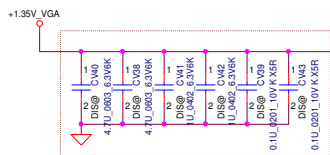


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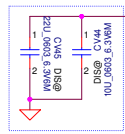
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Place under GPU

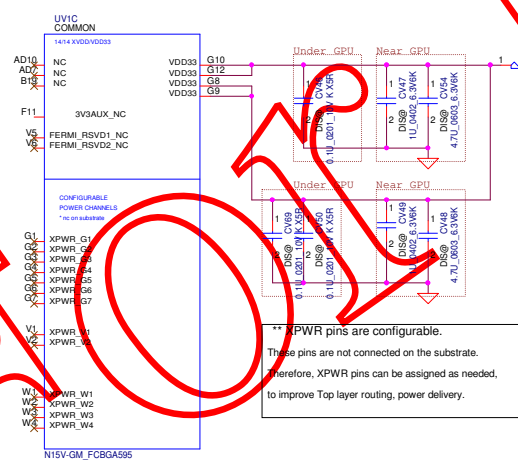
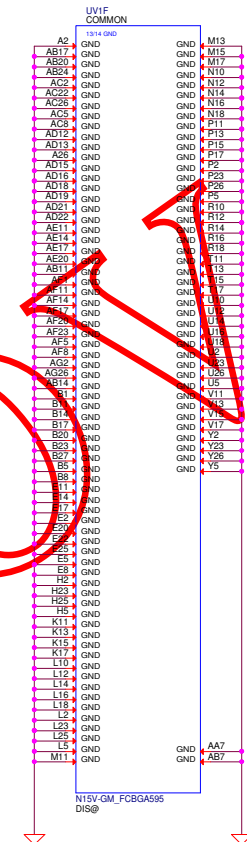
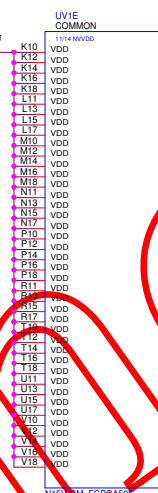


Place near GPU

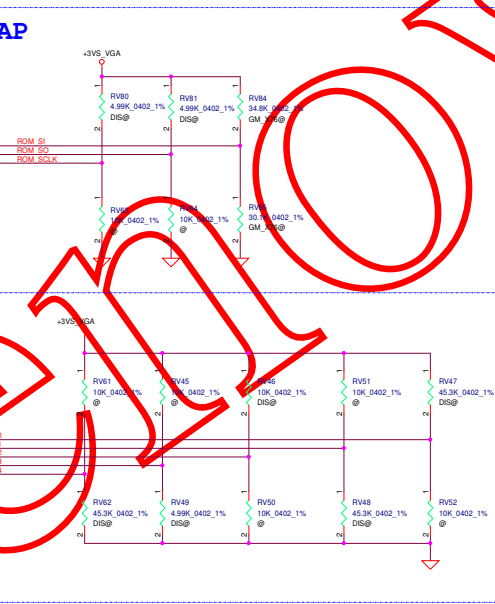
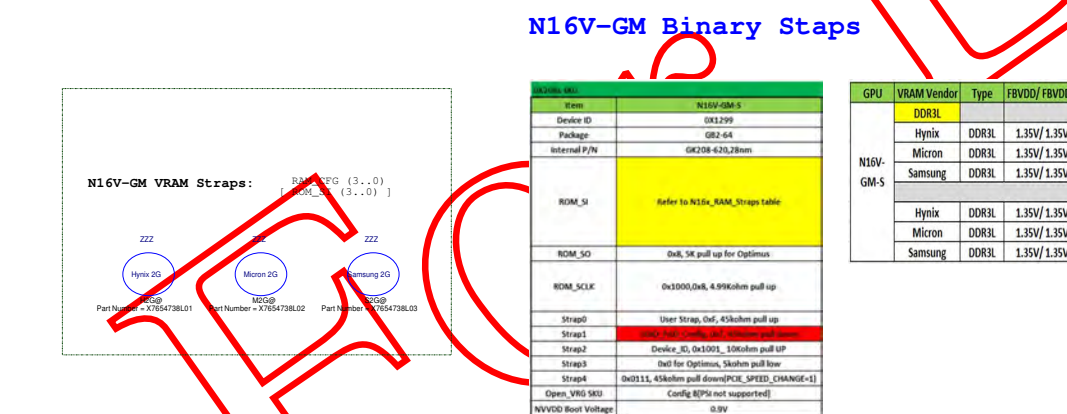
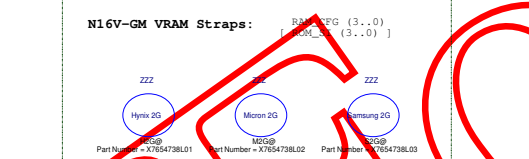


GPU_Decoupling
CAPs @ Power
Page

+VGA CORE
Voltage by GPU SKU



**XPWR pins are configurable.
These pins are not connected on the substrate.
Therefore, XPWR pins can be assigned as needed,
to improve Top layer routing, power delivery.

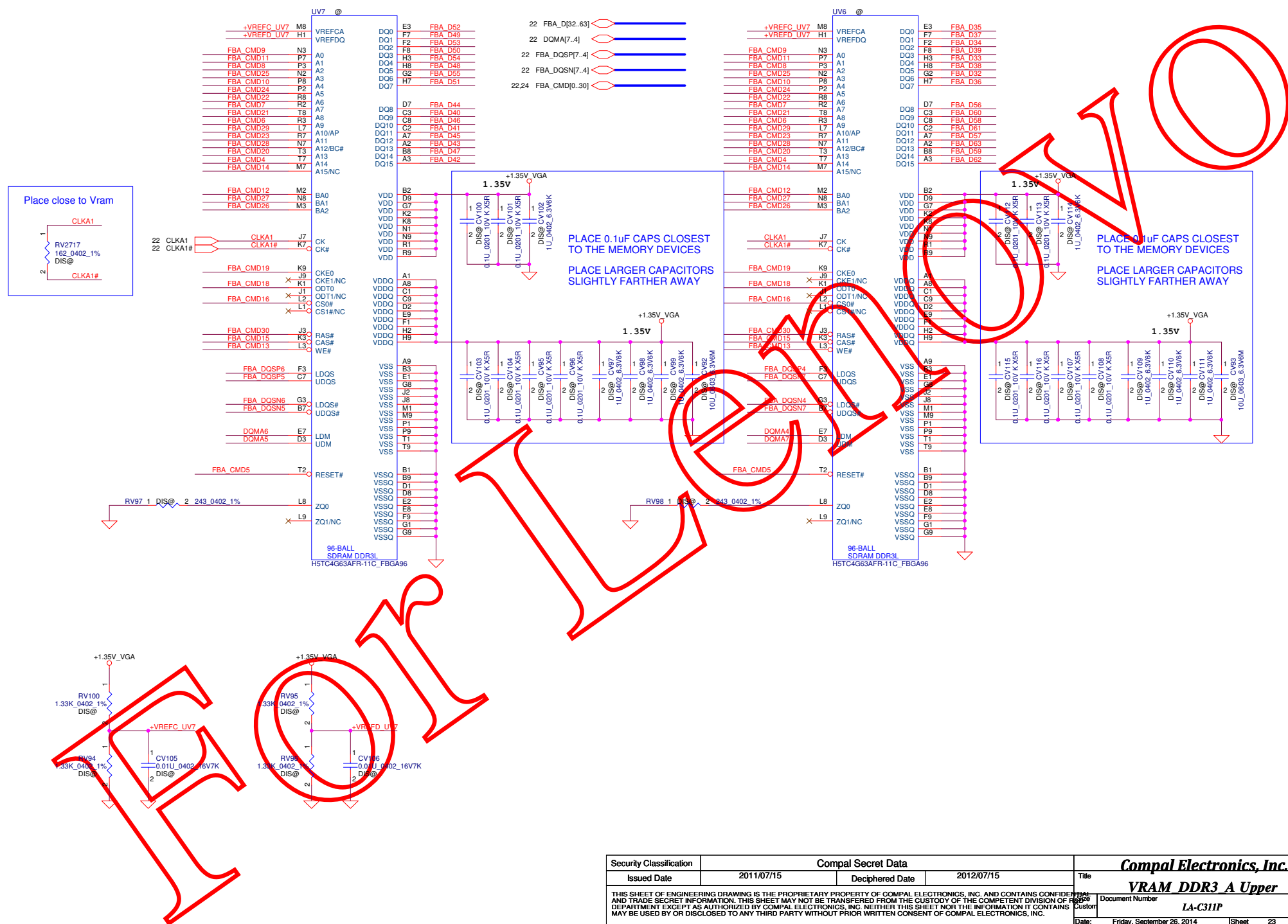


N150-MSU	
Item	N150-MSM5
Device ID	0X1299
Package	GR2-64
Internal P/N	GR208-620,78mm
ROM_S1	Refer to N15x_RAM_Straps Table
ROM_S0	0x6, 5K pull up for Optimus
ROM_SCLK	0x1000, 4.99Kohm pull up
Strap0	User Strap, 0x6, 43kohm pull up
Strap1	Device_ID, 0x1011, 10kohm pull up
Strap2	Device_ID, 0x1011, 10kohm pull up
Strap3	Dev for Optimus, 5kohm pull up
Strap4	0x0111, 45kohm pull down(PCEI_SPEED_CHANGE=1)
Open_VBIO_SKU	Config BPS not supported
NVDDIO Pull Voltage	0.9V

GPU	VRAM Vendor	Type	FBVDD/ FBVDDQ	Memory Density	Configuration	VRAM P/N	Max Speed CLK	D/C Mini	Die-Revision	RAM_CFG	ROM_SI	Status
N16V-GM-S		DDR3L			Single Rank or Single Rank							
	Hynix	DDR3L	1.35V / 1.35V	128Mx16		H5TCG63FFR-11C	900Mhz	NA	F-Die	0x8	PU 20K	Production ready
	Micron	DDR3L	1.35V / 1.35V	128Mx16		MT41J128M16T-093G-X	900Mhz	1322	K-Die	0x8	PU 4.99K	Production ready
	Samsung	DDR3L	1.35V / 1.35V	128Mx16		K4W2G1646Q-BC1A	900Mhz	NA	Q-die	0x7	PD 45.3K	Production ready
					Dual Rank							
	Hynix	DDR3L	1.35V / 1.35V	256Mx16		H5TCG63AFR-11C	900Mhz	NA	A-Die	0xE	PU 34.8K	Production ready
	Micron	DDR3L	1.35V / 1.35V	256Mx16		MT41J256G16HA-093G-E	900Mhz	NA	E-die	0xD	PU 30.1K	Production ready
	Samsung	DDR3L	1.35V / 1.35V	256Mx16		K4W4K61646Q-BC1A	900Mhz	NA	D-Die	0x5	PD 30.1K	Production ready

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Size	A		Revision	LA-311P

Memory Partition A - Upper 32 bits [64..32]



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Memory Partition A - Lower 32 bits [31..0]

Table 6-3 lists the Mode D command mapping and Table 6-4 on page 91 lists Mode E.

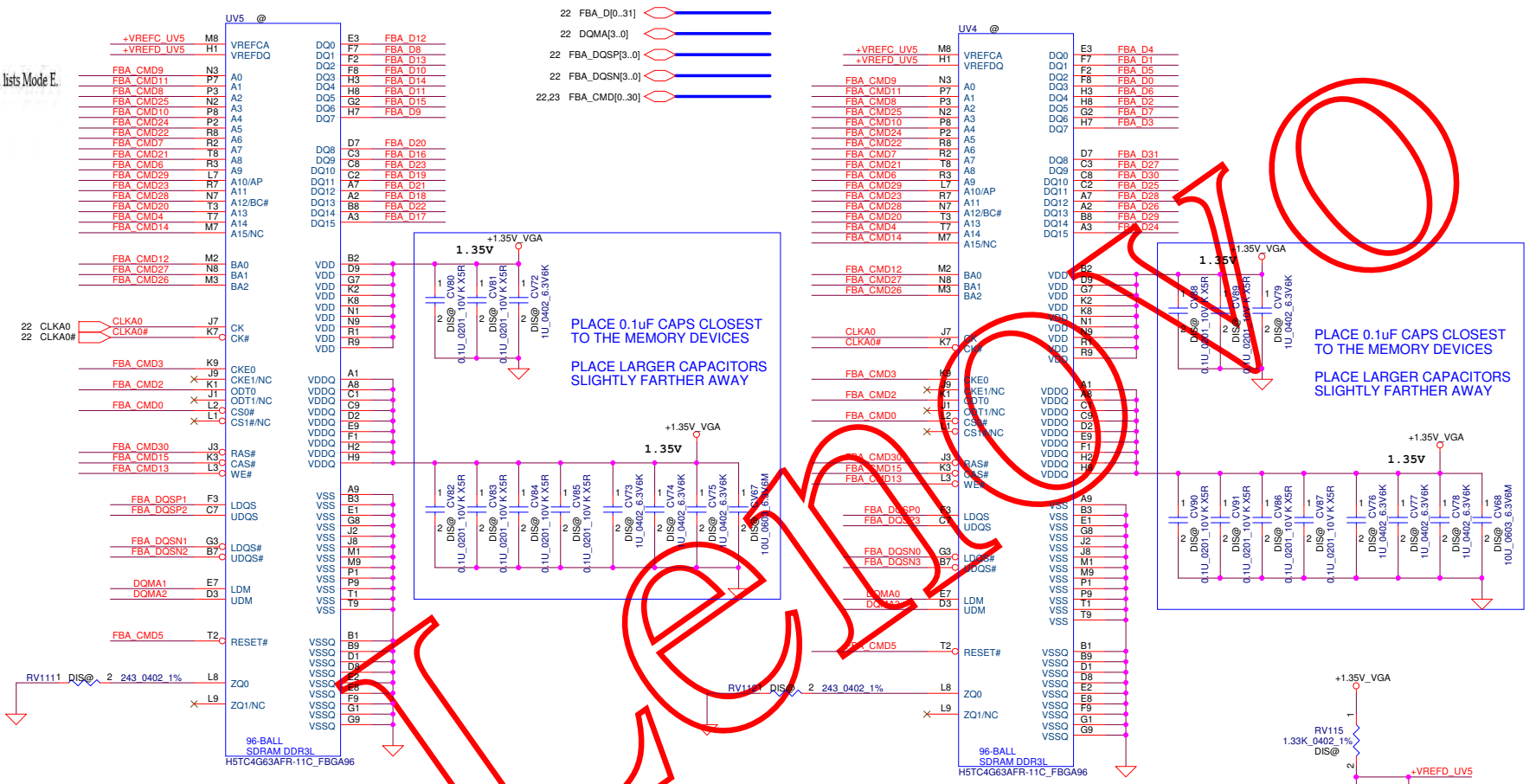
Table 6-3. Mode D Command Mapping

N15x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*

N15x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD16		CS0*
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS*	RAS*
FBx_CMD31		
FBx_CMD32		
FBx_CMD33 ¹		
FBx_CMD34	DBG0 ²	
FBx_CMD35	DBG1 ²	

Notes:
1. Not available in GB2B-64 package.
2. GPU debug pins; not connected to DRAM. See section 6.1.11

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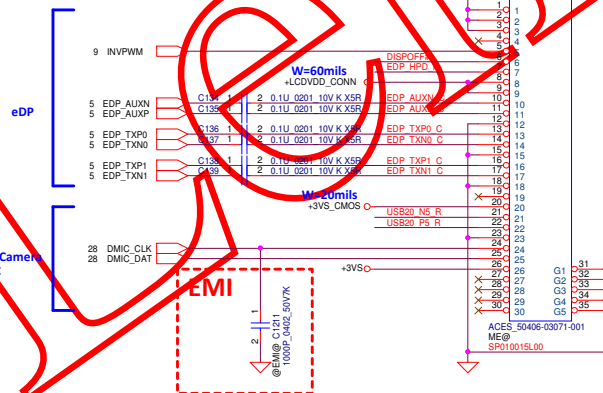
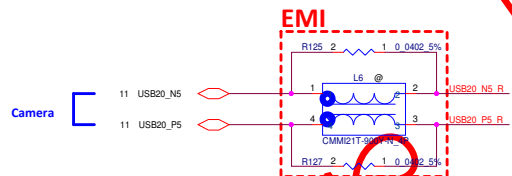
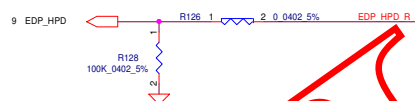
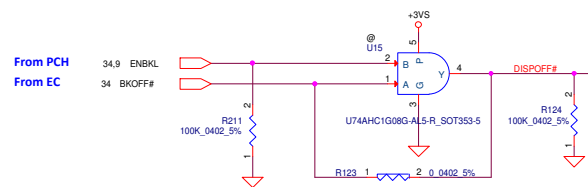
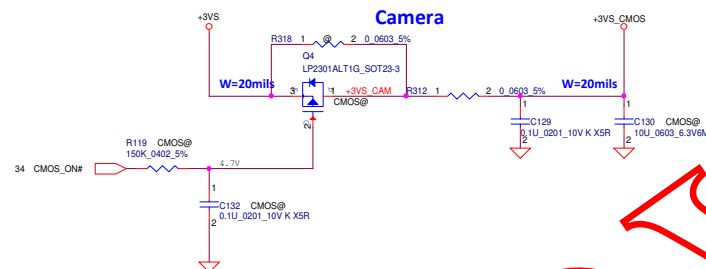
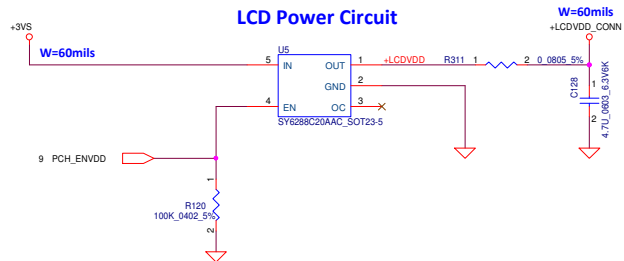
6.1.3 DDR3 Frame Buffer Command Mapping

N15x GPUs have generic FBx_CMD[35:0] pins that connect to the memory command/address pins. To optimize the layout for different memory types and packages, the GPU's support different mapping modes (Table 6-2). Choosing the best command mapping will help simplify layout and allow you to reduce layer count and/or area.

Table 6-2. Support Command Mapping by GPU Package

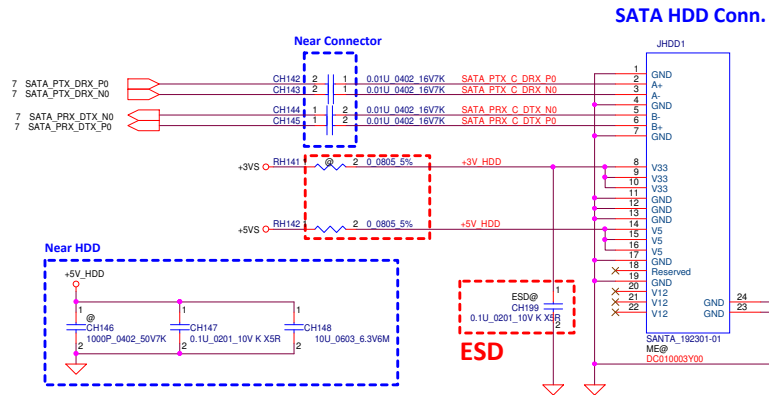
Packages	Supported CMD Mapping for DDR3	Benefits
GB2B-64 GB4B-128	D	Mode D is optimized for N15x using DDR3 memory in the BGA96 package and is supported for single rank designs. Using this mode will allow routing in four signal layers ¹ . This compact layout offers a high level of symmetry allowing higher speeds without requiring termination.
GB2B-64 GB4B-128	E	Mode E is optimized for DDR3 dual rank designs.

Note: ¹not including two additional layers for power planes.

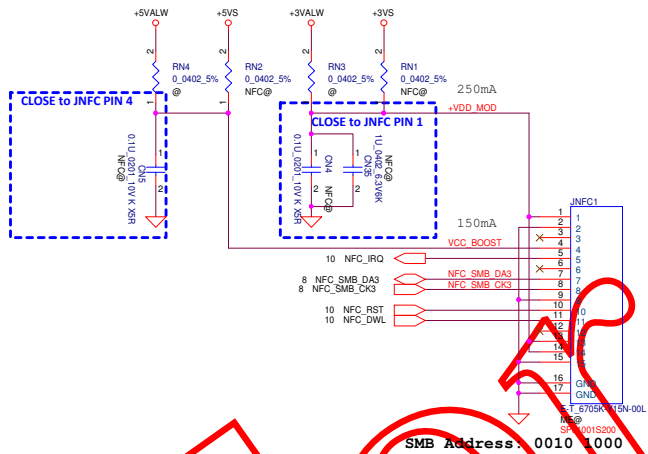


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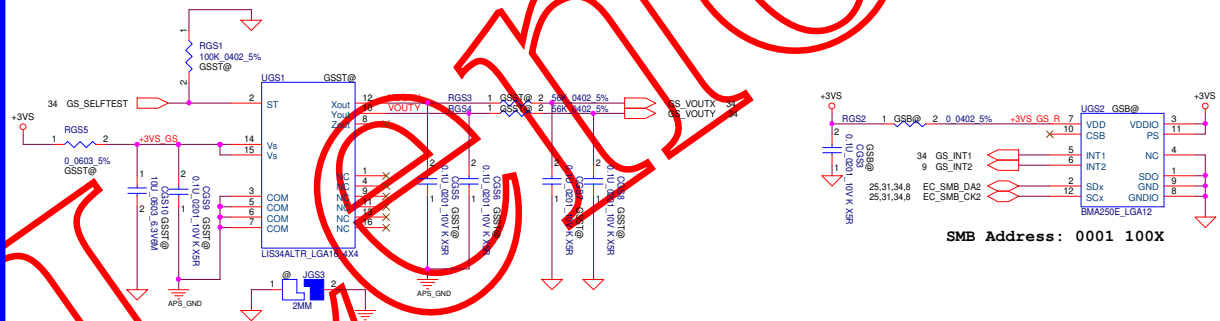
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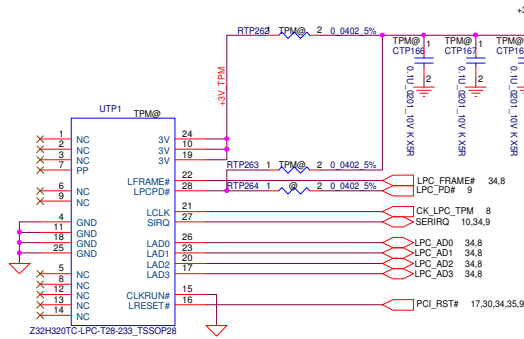
NFC



APS (G-Sensor)



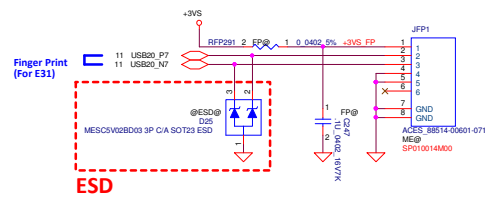
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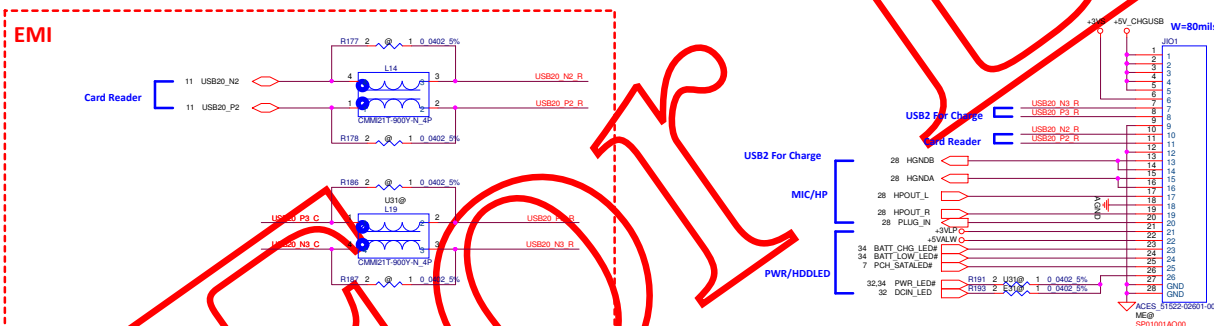
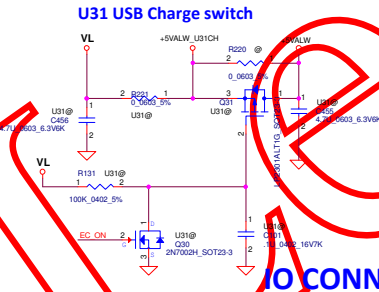
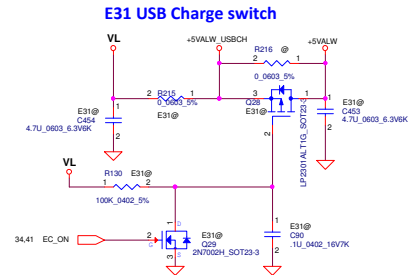
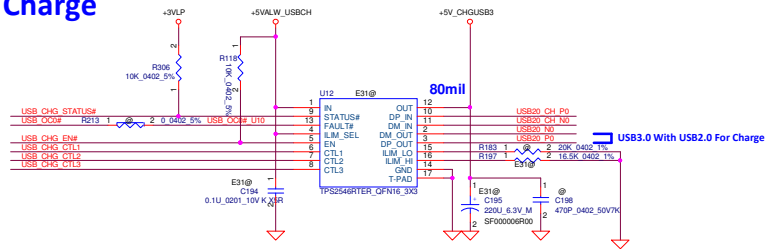
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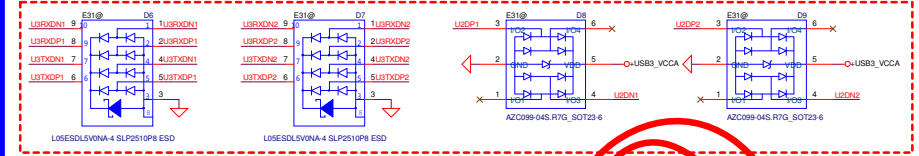
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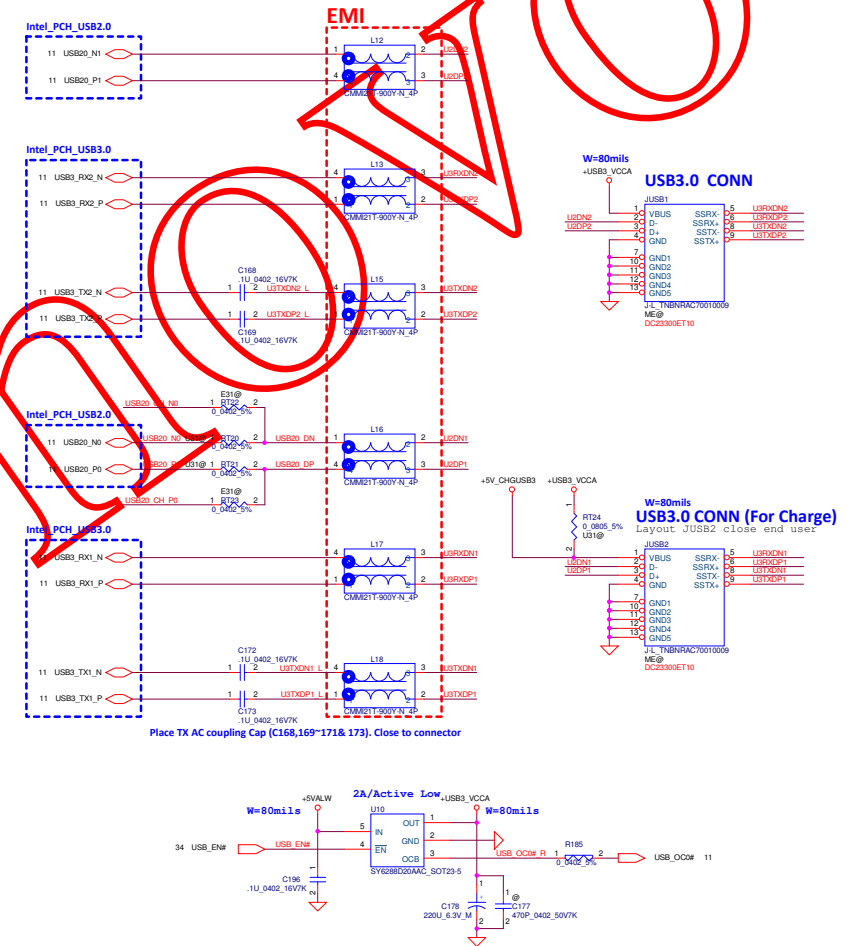
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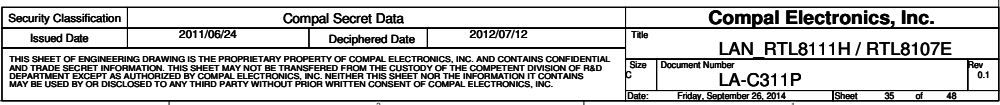
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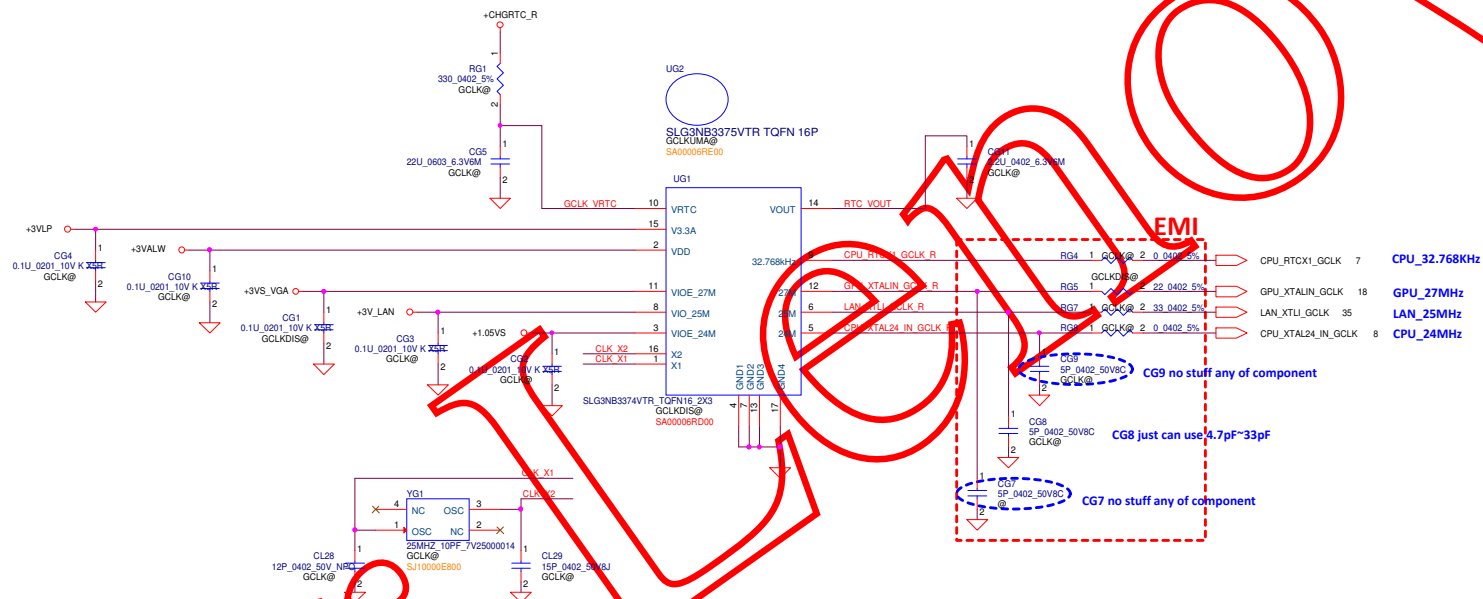


USB3.0_Port



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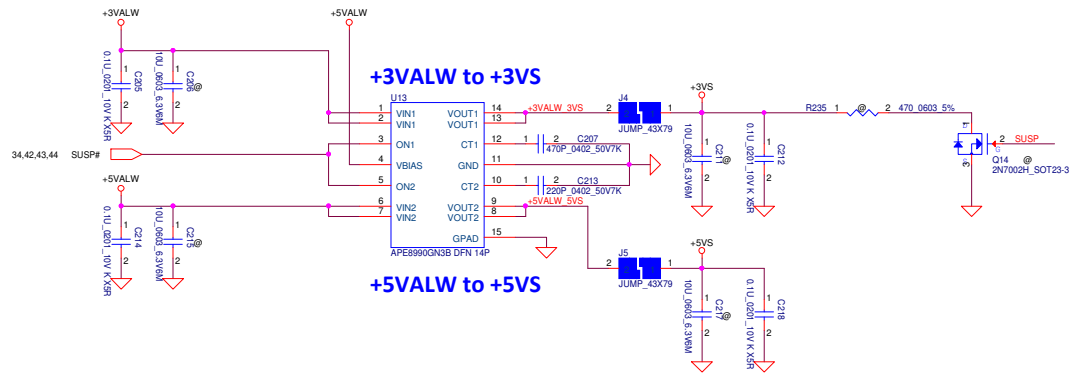




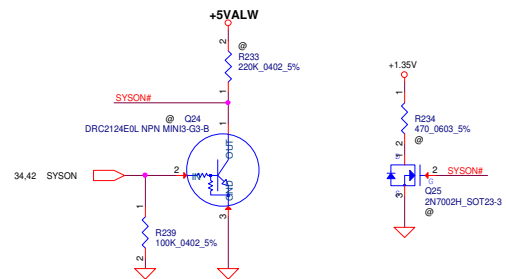
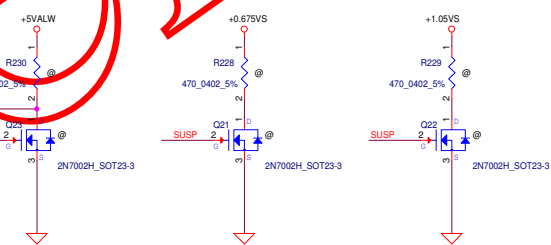
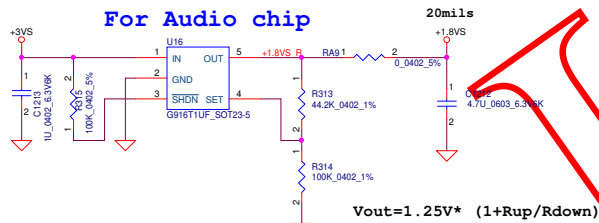
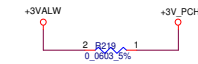
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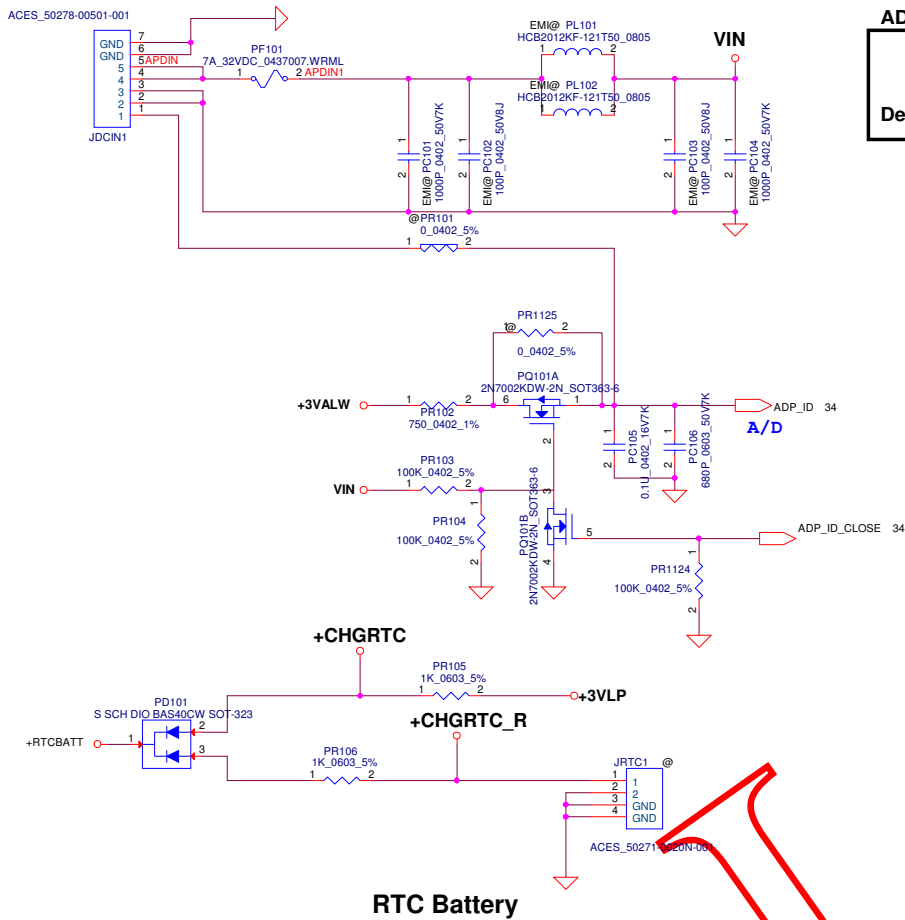
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+3VALW to +3VALW_PCH



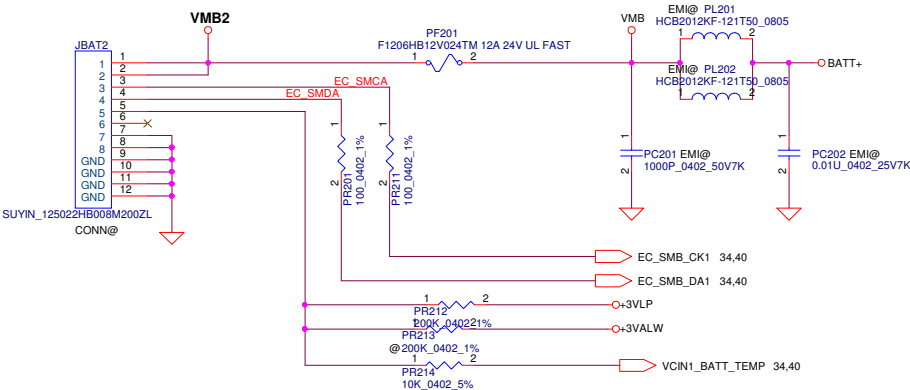
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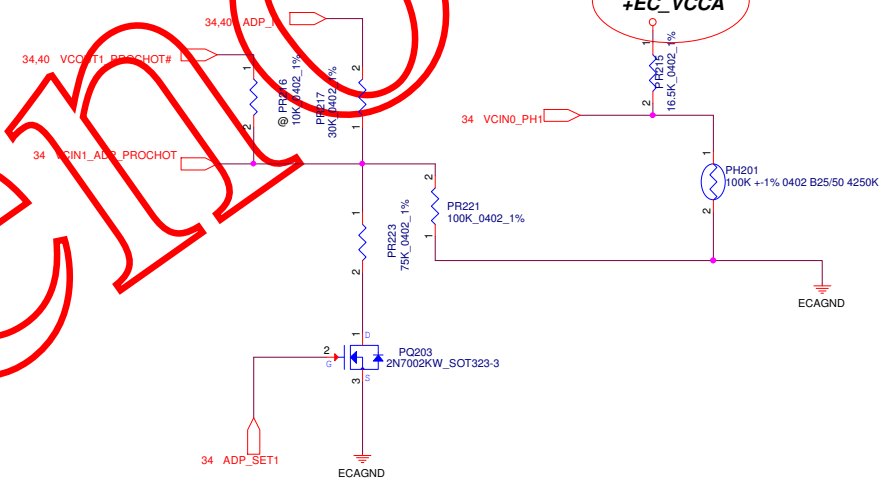
ADP_ID	AC Adapter	90W	65W
R(K ohm)	open	10	
ADP_ID(V)	3.3	1.65	
Detection voltage	>2.64	1.32~1.98	

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PH201 under CPU bottom side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



20120314
Change to +EC_VCCA from +3VLP

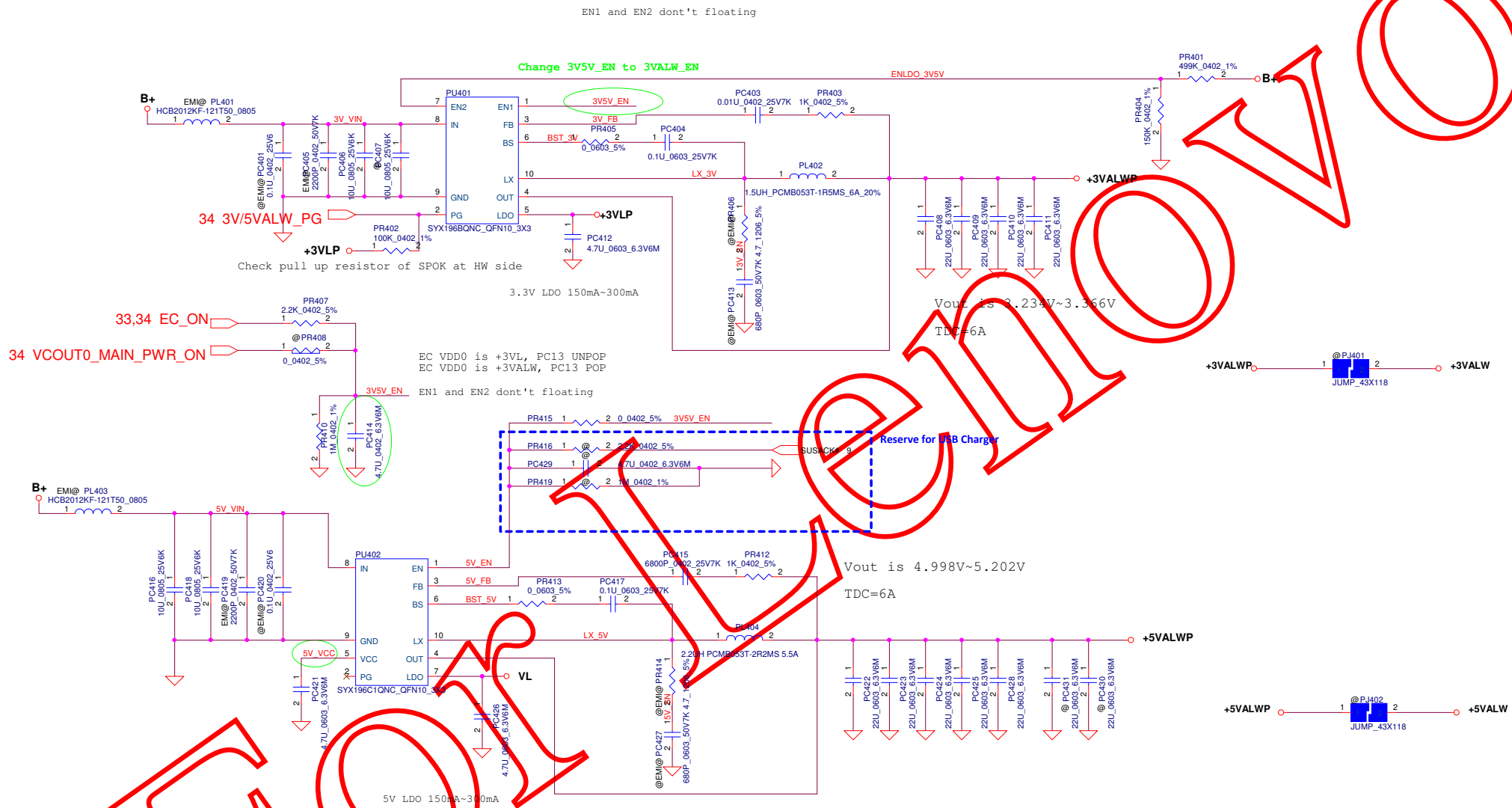
+EC_VCCA

FOR LAYOUT

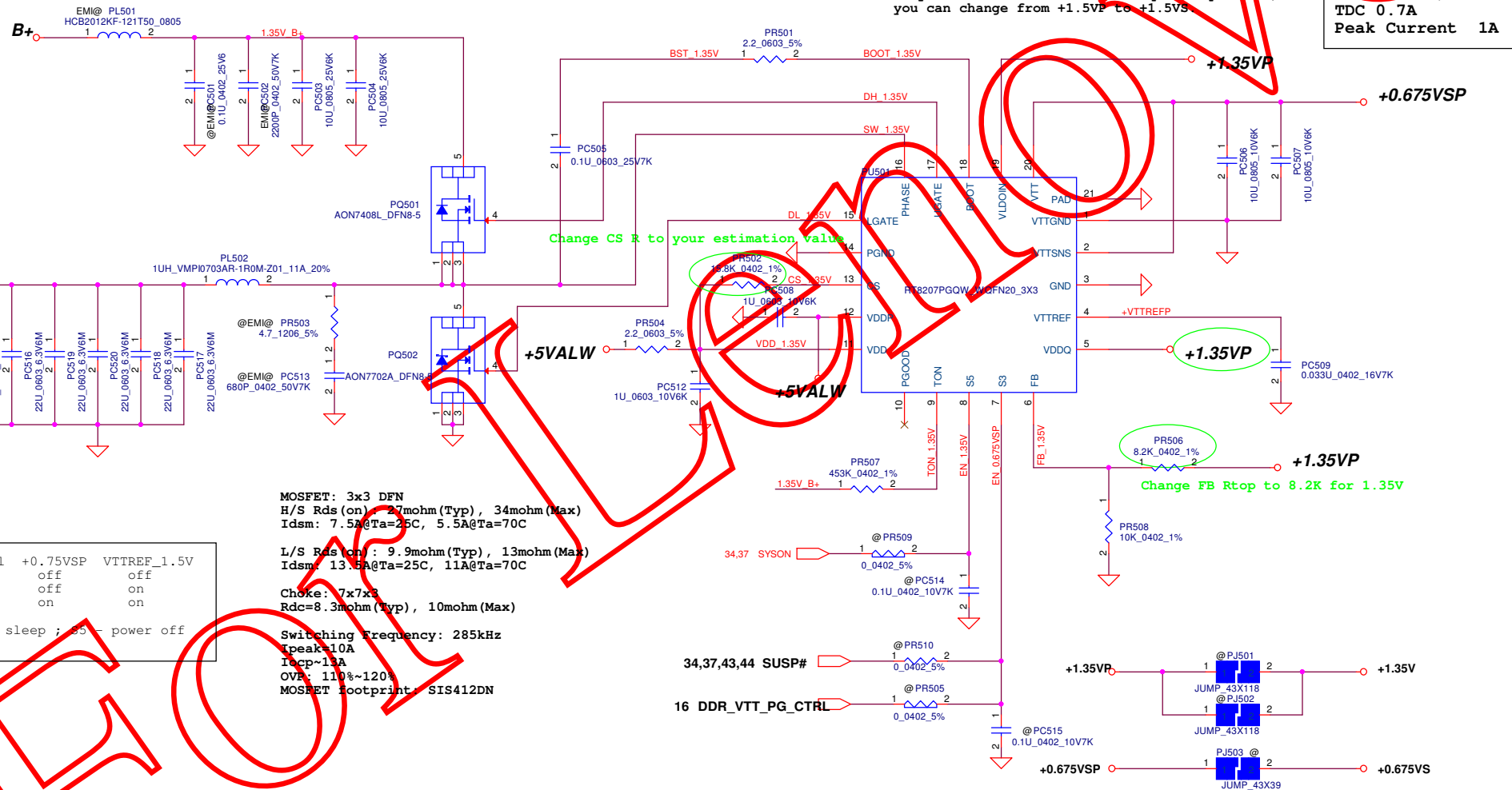
135W : 150W(Turbo_V=1.2) active 135W(Turbo_V=1.072) recovery
90W : 100W(Turbo_V=1.2) active 90W(Turbo_V=0.903) recovery
65W : 70W(Turbo_V=1.2) active 65W(Turbo_V=0.918) recovery
45W : 65W(Turbo_V=1.2) active 45W(Turbo_V=0.829) recovery

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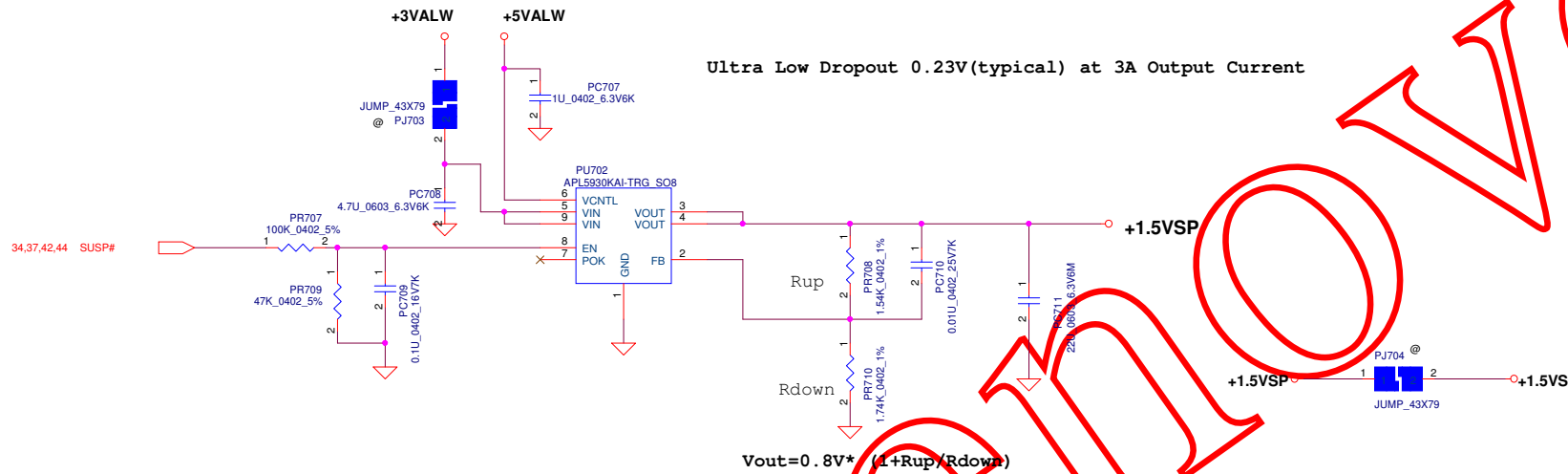




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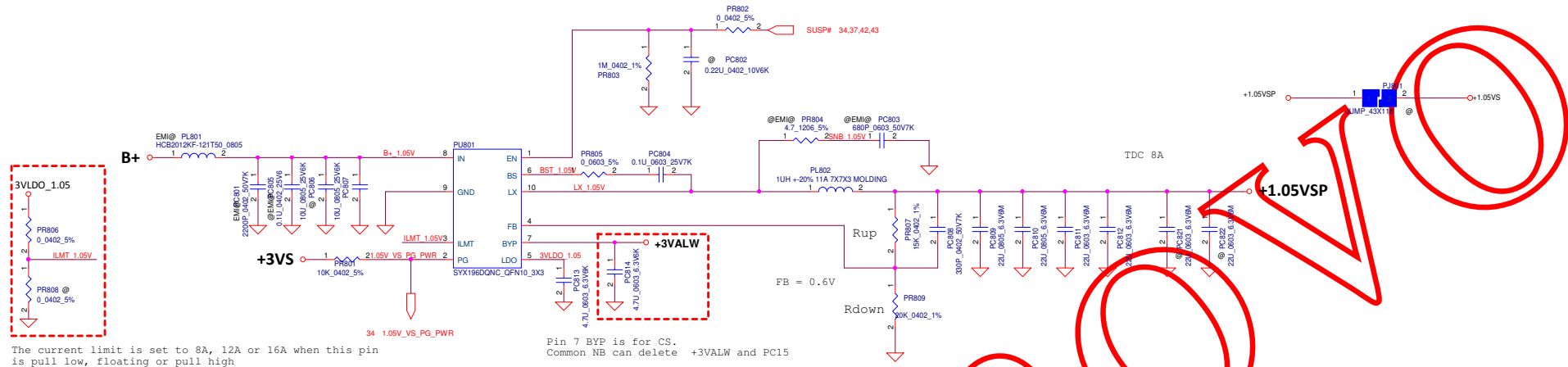


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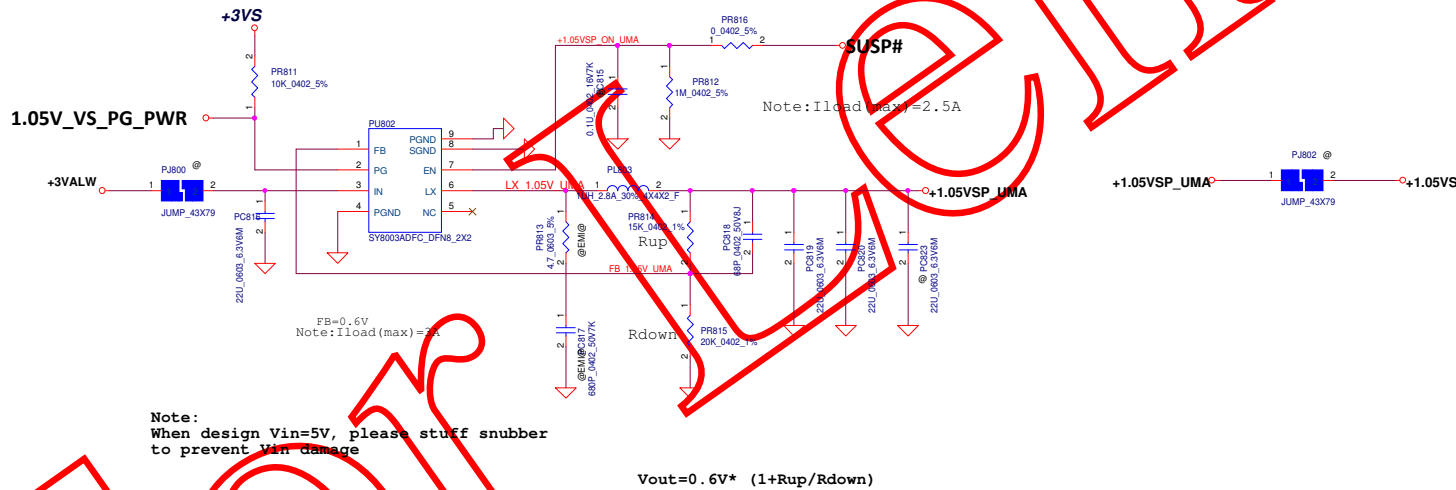
EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

$$V_{FB} = 0.6V$$
$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$
$$V_{out} = 1.05V$$



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

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Base on BDW PDDG Rev_0_73

Location	15W	Note
	TDC 14A MAX 32A OCP 39A Loadline=-2.0mV/A	
PR1120	499 Ohm	OCP
PR537	1.27kOhm	Droop
PC528	0.022uF	RC Match
PR507	90.9kOhm	PROG1
PR703	93.1kOhm	IMON
PC518	0.1uF (0402)	RC Filter

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

Choke: 0.12uH (Size:7*7*4)
Rdc=0.62mohm +5%
Heat Rating Current=4.5A
Saturation Current=41A

+1.05VS

Follow intel guideline

Note:
VR_SVID_ALRT# Pull high on HW side

12 VR_SVID_DAT

12 VR_SVID_ALRT#

12 VR_SVID_CLK

12 VR_ON

12 VGATE

Note:
VR_HOT# Pull high on HW side

34 VR_HOT#

Over temperature protection:
OTP Setting: 100C active
Pin5 (NTC) voltage <0.88V, Protect
Pin5 (NTC) voltage >0.92v, recovery

Note:
PR1104=169K
=>Icc(max)=33A
fsw=700KHz

+5VS

Note:
PR1112=124K
=>Slew rate=53mV/us
Vboot = 1.7V

RC Match

OCP Setting

Local sense put on HW site

CPU_B+

B+

+CPU_CORE



123

File
ISL95813 for BDW-Y&U(15W/28W) CPU

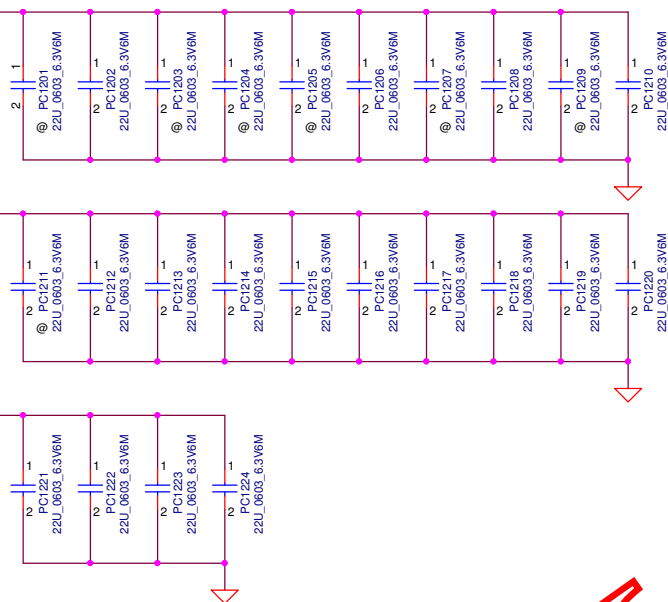
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+CPU_CORE

24 X 22u/0603



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Remark:

1. Switching frequency setting: (Ton pin)
 $F_{sw} = (V_{in} - 0.5) / (2 \cdot V_{in} \cdot R_{ton} \cdot 3.2\pi) = 448\text{KHz}$

2. Soft-Start: (SS pin)
SS time (Internal) is 0.7ms (PC18 un-pop)
SS time (External): (PC18 pop)
 $T_{ss} = (C_{ss} \cdot V_{refin}) / I_{ss} + 2.3\text{ms} = 0.01\mu\text{F} \cdot 0.9\text{V} / 5\mu\text{A} + 2.3\text{ms} = 4.1\text{ms}$

3. PWM-VID Spec and component Values

PWM-VID Spec	Config A	Config B
Vmin	0.6V	0.6V
Vmax	1.2V	1.2V
Vboot	0.875V	0.9V
Voltage step	6.25mV	6.25mV
N of Voltage level	96	96
Rrefadj	PR806 39K	20K
Rref1	PR803 39K	20K
Rboot	PR805 1.5K	2K
Rref2=PR20+PR21	PR809 30K	18K
	PR812 1.5K	0
C	PC829 1.5nf	2.7nf

$V_{boot} = V_{ref} \cdot R_{ref2} / (R_{ref1} + R_{ref2} + R_{boot})$
 $R_t = R_{refadj} // (R_{boot} + R_{ref2})$
 $V_{min} = V_{ref} \cdot R_{ref2} / ((R_{ref1} // R_{ref2}) + R_{boot} + R_{ref2})$
 $V_{max} = V_{ref} \cdot R_{ref2} / ((R_{ref1} // R_{ref2}) + R_{boot} + R_{ref2})$
 $V_{out} = V_{min} + N \cdot V_{step}$
 $V_{step} = (V_{max} - V_{min}) / N_{max}$

4. Current Limit threshold setting
 $R_{ocset} = (I_{valley} \cdot R_{ds(on)} + 40\text{ mV}) / 10\mu\text{A}$
 $I_{ripple} = (20 - 1.028) \cdot 1.028 / (448\text{KHz} \cdot 0.22\mu\text{F} \cdot 20) = 9.89\text{A}$

OCP=54A/2=27A per phase
 $I_{valley} = 27\text{A} - 9.89\text{A} \cdot 2 = 22.055\text{A}$

H-side MOS: TPCA8065 L-side MOS: TPCA8057
 $R_{ds(on)}$:
11.7mohm@Vgs=10V 2.0mohm@Vgs=10V
9.4mohm@Vgs=4.5V 2.6~3.2mohm@Vgs=4.5V
 I_d : 16A@Ta=25 degC I_d : 42A@Ta=25 degC

Choke: 0.36uH (Size: 10*10*4)
 $R_{dc} = 1.1\text{mohm} \pm 5\%$
Heat Rating Current=30A
Saturation Current=50A

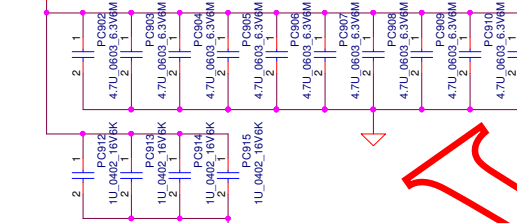
C=3*330uF (9mohm)=990uF
 $V_{ripple} = I_{ripple} \cdot ESR(\text{min}) = 9.89\text{A} \cdot 3\text{mohm} = 29.67\text{mV}$

5. OpenVReg Configurations: (PSI pin)

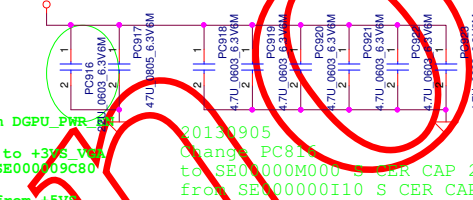
Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	20130909
Active phase with CCM	1. Change net name to GPU_PWR_EN from DGPU_PWR_EN

2. Unpop PR801 0.0402 5%
3. Add PR824 10K 0402 5% to pull high to +3VS_VGA
4. Reserve PC834 5600P_0402_50V7K SE00009C80
20131024
1. Change PR814 pull high to +5VALWS from +5V

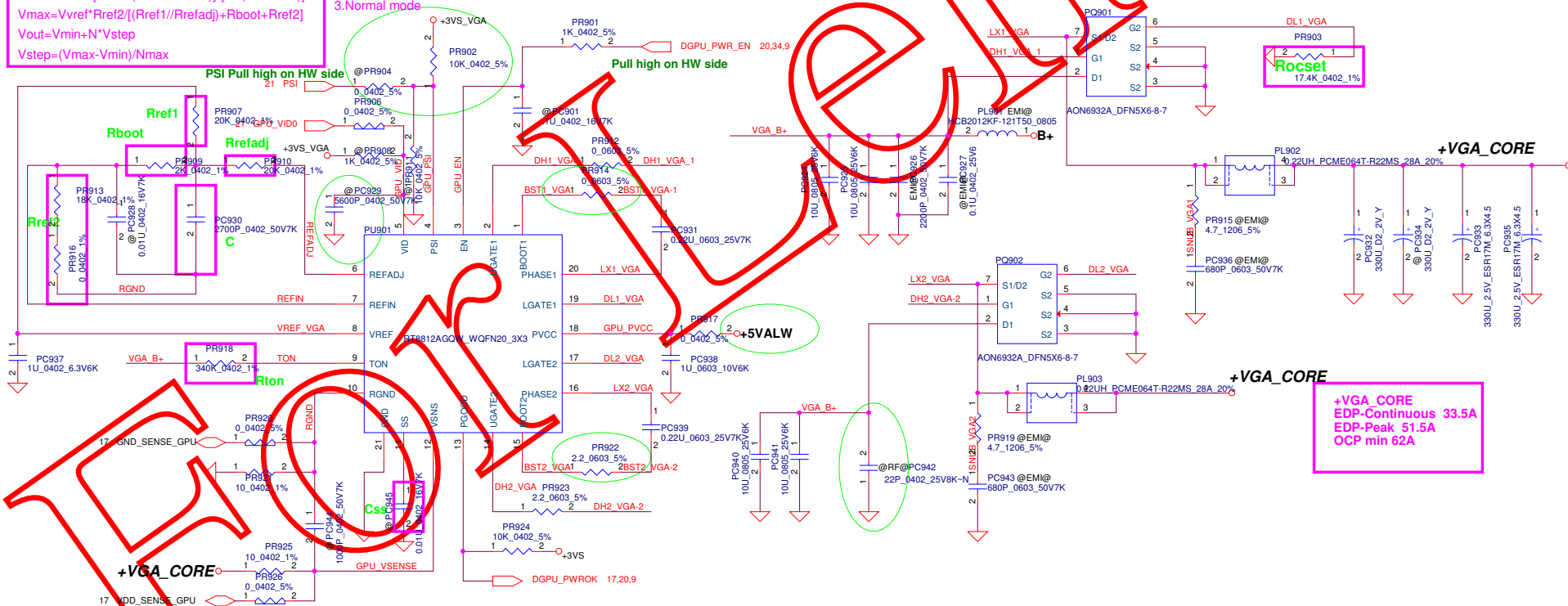
+VGA_CORE Under GPU Core GB2-64 package



+VGA_CORE Near GPU Core



20130905
Change PC815 to SE00000M000 5 CER CAP 22uF 6.3V M X5R 0603
from SE000000I10 S CER CAP 22uF 6.3V M X5R 0805 H1.25



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